4 3 2 1

D C B A

AD0 AD1 AD2 AD3 AD4 AD5

CE'1 0110 0111A

R/W R/W R/W

ENABLE ENABLE ENABLE

H1 DATACLK H1

L1 L1

A11 A12 A13 A14 A15

R/W DATACLK 0110 ENABLE R/W

ESC1 ESC2 SRAC1 SRAC2 EAC1 EAC2

R/W DATACLK 0111A ENABLE R/W

C0 C1 C2 C3

20MHZ X1 X2

'LS163

2.5MHZ

CLK

C3 ENABLE

CE'6 CE'1 CE'4 ESC1 CE'5 ESC2

L1

LS197 LS197 LS197

ENABLE DESEL CE'5

ENABLE DESEL CE'4

CLK H1 DESEL

SRAC1 SRAC2

ENABLE CE3

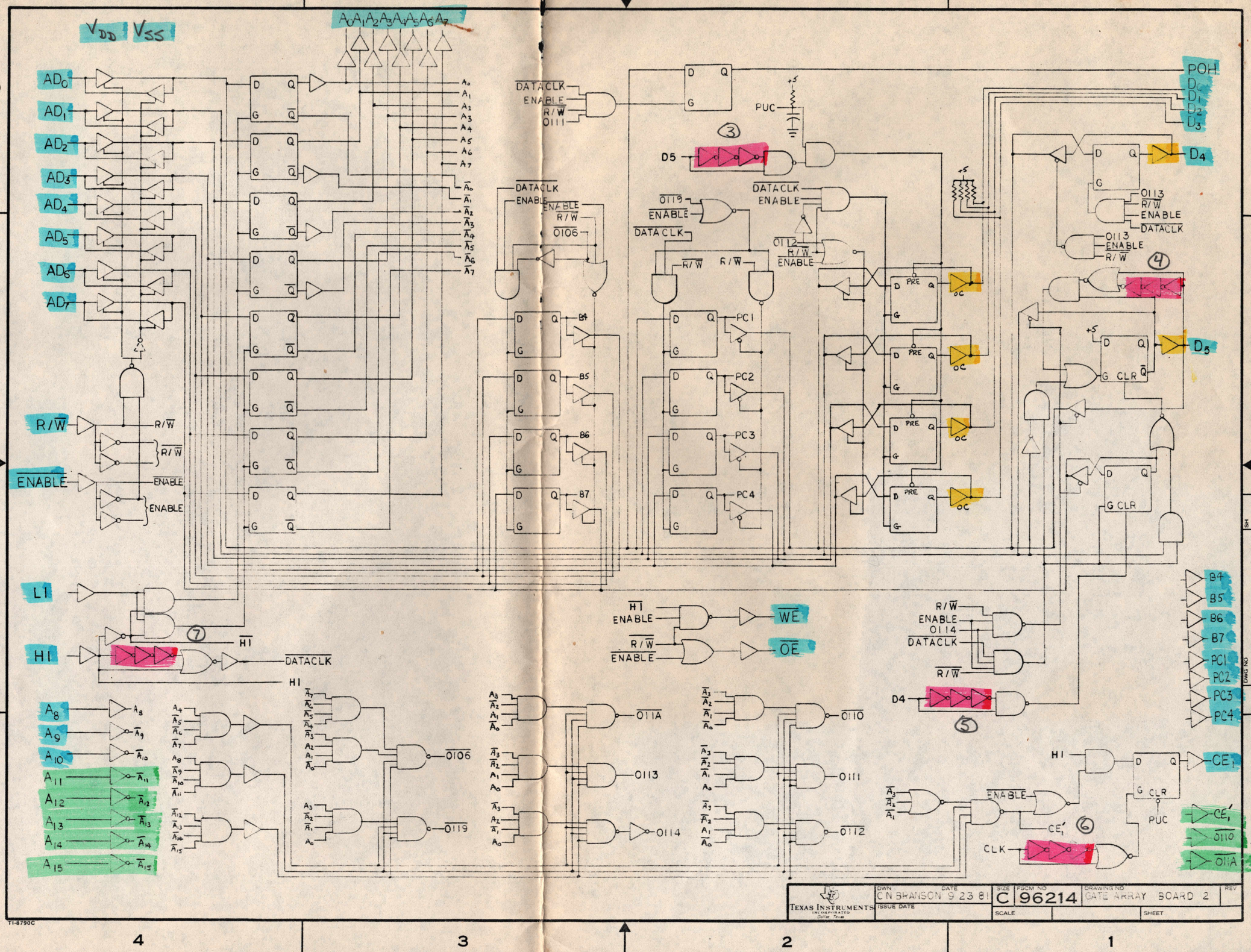
ENABLE CE2

ENABLE DESEL CE6

CE1 CE2 CE3 CE4 CE5 CE6

TI-8790C

| | | | | |
|---|---|---|---|---|
| Texas Instruments Incorporated, Dallas, Texas | DWN C N BRANSON 9-23-81 | SIZE C | FSCM NO 96214 | DRAWING NO GATE ARRAY BOARD 1 |
| | ISSUE DATE | SCALE | | SHEET |


4
3
2
1
D
C
B
A
$V_{DD}$ $V_{SS}$
$A_0A_1A_2A_3A_4A_5A_6A_7$
$AD_0$ $AD_1$ $AD_2$ $AD_3$ $AD_4$ $AD_5$ $AD_6$ $AD_7$
R/$\overline{W}$
ENABLE
L1
H1
DATACLK
$\overline{H1}$
$A_8$ $A_9$ $A_{10}$ $A_{11}$ $A_{12}$ $A_{13}$ $A_{14}$ $A_{15}$
$\overline{0106}$
$\overline{0119}$
$\overline{0111A}$
$\overline{0113}$
$\overline{0114}$
$\overline{0110}$
$\overline{0111}$
$\overline{0112}$
B4 B5 B6 B7
PC1 PC2 PC3 PC4
PUC
D5
D4
$\overline{WE}$
$\overline{OE}$
POH $D_0$ $D_1$ $D_2$ $D_3$
$D_4$
$D_5$
$CE_1$
$CE_1'$
CLK
PRE
OC
CLR
TEXAS INSTRUMENTS INCORPORATED Dallas, Texas
DWN C N BRANSON DATE 9 23 81
ISSUE DATE
SIZE C FSCM NO 96214
DRAWING NO GATE ARRAY BOARD 2
REV
SCALE
SHEET
TI-8790C

# LSCU 1

## PRELIMINARY SPECIFICATIONS

## FOR VENDOR QUOTES

Texas Instruments
Consumer Products Group

10/12/81

# SECTION 1

# General Information

## 1.1 Quote Breakdown

Quotes are requested for Gate Array / Semi-Custom CMOS implementation of the logic provided. Expected volume requirements are indicated below. Package information is given in Section 2. Quotes are requested for the preferred package and invited for any alternate packages. The logic provided should be referred to as LSCU 1. A quote is also requested for a modification of this logic, referred to as LSCU 1-A. This modification reduces pin out requirements by eliminating latches and outputs associated with PC2, PC3, & PC4, and eliminating the use of A9, and A10 everywhere they appear in the logic (all other logic remains as shown in the diagrams).

## 1.2 Volume

* Packaged prototype units required by April 1, 1982
* First production 2H82: 10,000 - 20,000 units
* Production: 1Q83 - 20,000 units
  2Q83 - 30,000 units
  3Q83 - 50,000 units
  4Q83 - 20,000 units

## 1.3 For Additional Information

For clarification or additional information contact

Chuck Branson
Design Engineer, Consumer Products Group
Texas Instruments, Inc.
P.O. Box 10508, M/S 5889
Lubbock, TX 79408
(806) 741-3020

or

Randy Ahlfinger
Program Manager, Consumer Products Group
Texas Instruments, Inc.
P.O. Box 10508, M/S 5889
Lubbock, TX 79408
(806) 741-3215

# SECTION 2

# PACKAGES

## 2.1 Preferred Package

* Form - Quad Flat Pack
* Plastic
* Minimum Pin Count - 60
* Maximum Overall Size - 30 x 30 x 3 mm
* Leads Solderable
* Leads flush with bottom surface
* For example of package refer to the attached sheets

## 2.2 Other Packages (In order of acceptability)

* Pin Grid Array, RIT, Square pack
* LCC
* DIP

# SECTION 3

## Electrical Characteristics

1. Technology - CMOS

2. Operating Temperature Range - 0 C - ~~70 C~~ +70 C

3. Vdd - Min: Vss ~~4.5, Max: Vss 5.5~~ 4.3 - 5.8 MAX: Vss + 5.5

4. Inputs - Typical CMOS compatibility

5. Outputs - Typical CMOS compatibility except open drain outputs

6. Open drain outputs - capable of sinking 10 mA (prelim)

7. Power - less than 1 mW (dynamic, open drain outputs high)

8. Typical internal gate delay - 25 ns @ 5 V (see note)

NOTE

Critical paths are indicated on the logic diagrams and explained in Section 4

# SECTION 4

## Key to Color Coding on Logic Diagrams

Green – The diagrams were drawn for a two board, breadboard system. Some of the logic highlighted in green is duplicated due to the use of two boards and should only be built once. Three of the buffers highlighted in green are only for passing between the two boards and are not required at all in the final part.

Blue – Signals highlighted in blue indicate connections to I/O pads.

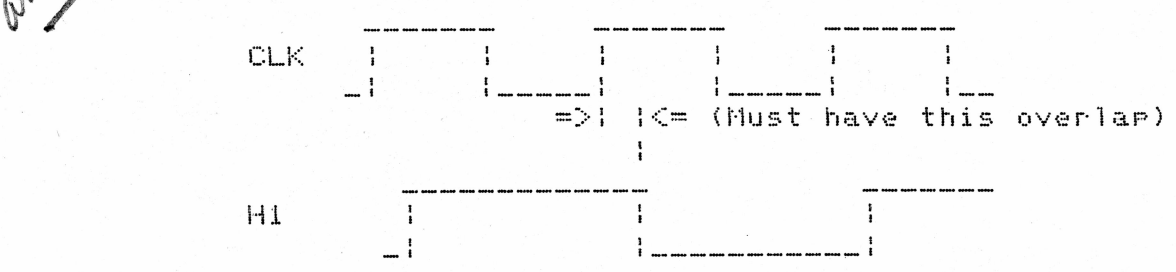
NOTE

If power-up-clear circuitry cannot be implemented on the chip then an additional pad will be required for this.

Yellow – Buffers highlighted in yellow are open-drain buffers.

Pink - Areas highlighted in pink indicate the paths which have been identified at this point as having critical timing requirements. The requirements are listed below.

1. DESEL is derived from CLK and H1. H1 is externally derived from CLK. There will be some small delay between CLK edges and H1 edges. The path between the CLK circuitry and the NOR gate input should be as short as possible to ensure that no glitch will will occur when CLK goes high and H1 goes low (see timing below).




In addition the delay between the NOR gate output and the signal indicated as DESEL should be approximately 100 ns.

2. Delay in this double edge detector should be approximately 50 ns.

3. Delay should be sufficient to preset the latches.

4. Delay should provide pulse capable of setting the latch.

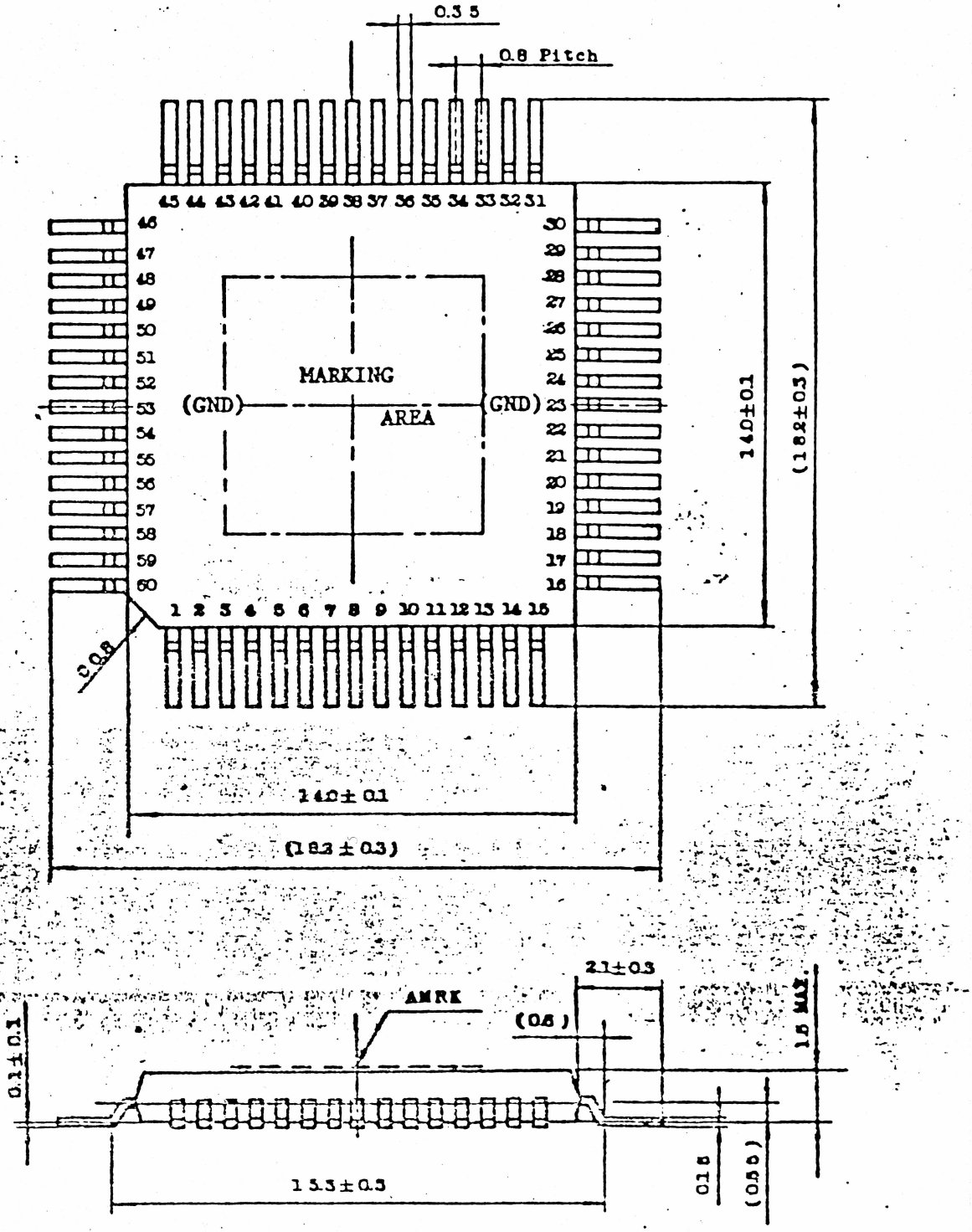
5. Delay should provide sufficiently wide pulse to clear the latch.

6. Delay should be sufficient to provide for opening the latch to the D input.

7. Delay should be enough to provide pulse capable of operating the latch gates.

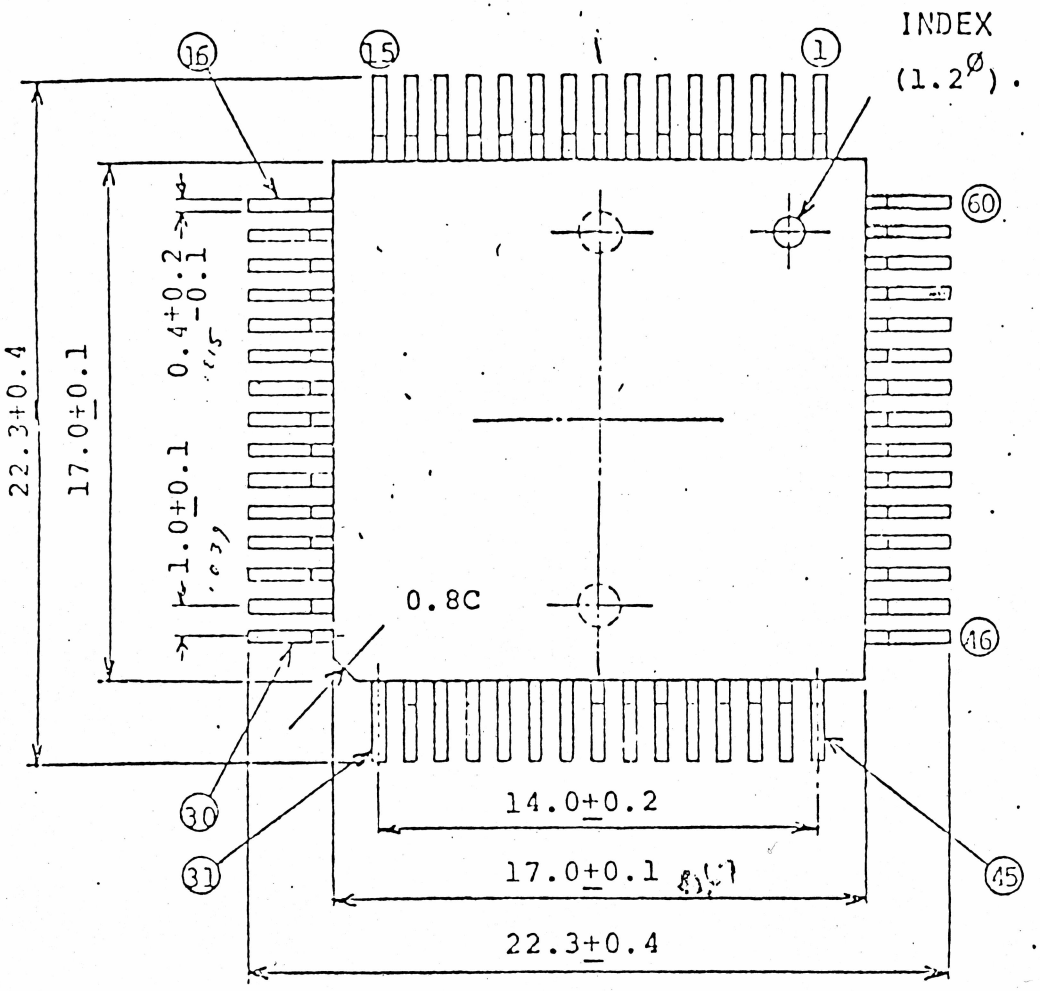
60 PIN MINI FLAT PACKAGE
(MEP 60-4 BS)

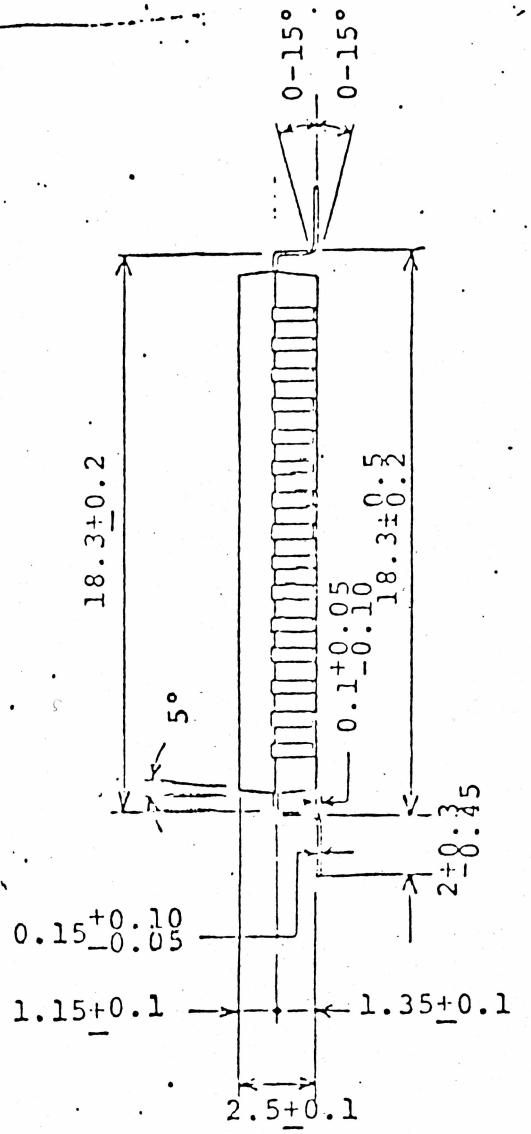
Unit in mm



60 PIN QUAD-IN-LINE PACKAGE

- FORMED LEAD -



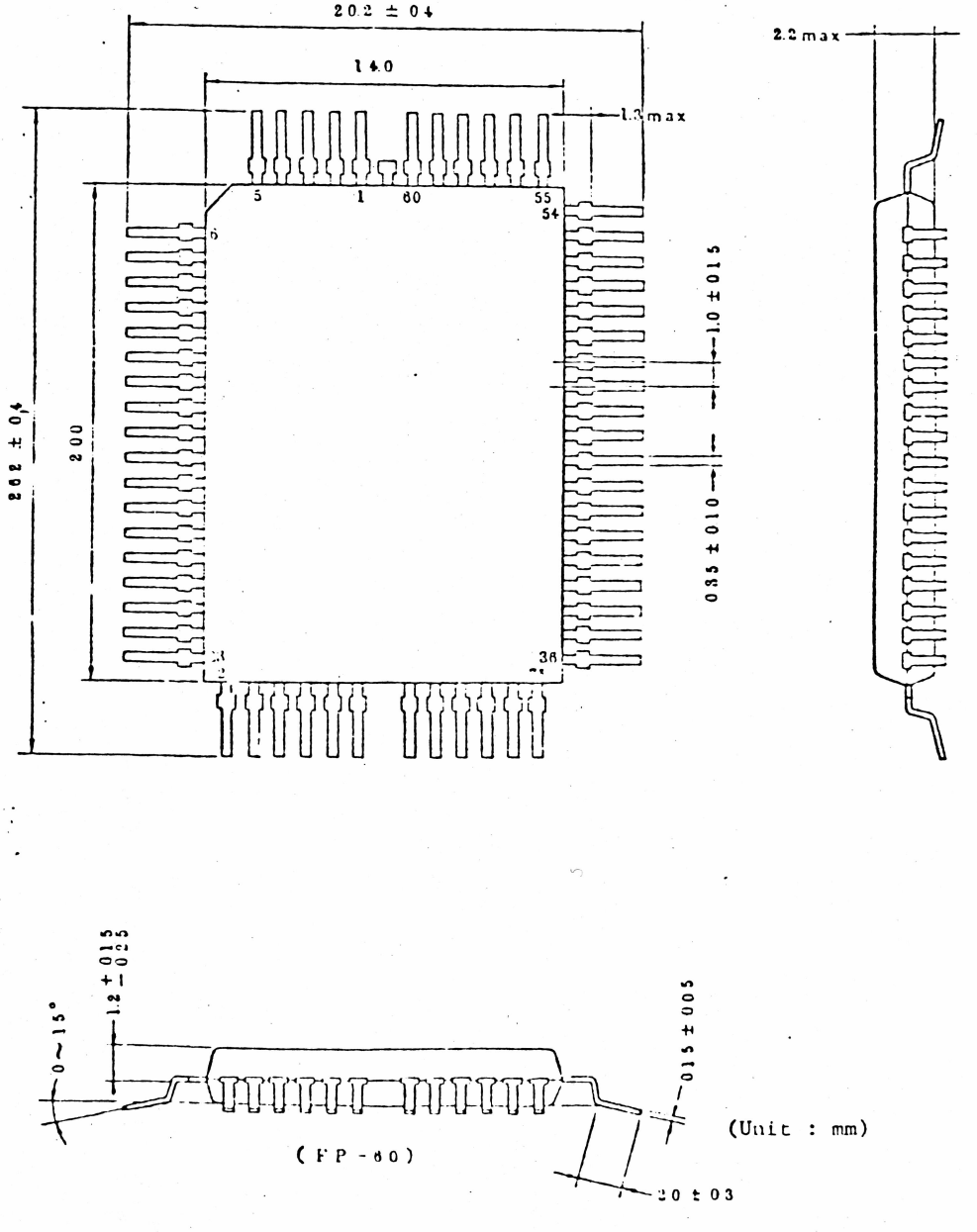




NOTE:- ALL DIMENSIONS ARE IN MM.

- EACH PIN CENTERLINE IS LOCATED WITHIN 0.2 OF ITS TRUE LONGITUDINAL POSITION
- LEAD THICKNESS IS AFTER TIN PLATING

(4) Diagram of Package Dimentional Outline

(60-pin Plastic Flat Package)




(FP-60)

(Unit : mm)